Amendments to the Claims

Kindly cancel claims 3-4, 7-11, 14-18, and 36-38 and amend claims 1-2, 5-6, 13, 25, and 29 as follows:

1. (currently amended) A pipelined microprocessor, comprising:

an instruction cache, configured to receive a fetch address on an address bus;

a branch target address cache (BTAC), coupled to said address bus, configured to provide a plurality of cached target addresses, ~~and~~ offsets, direction predictions, and valid indicators ~~in response to~~ indexed by said fetch address, wherein each of said plurality of cached target addresses, ~~and~~ offsets, direction predictions, and valid indicators is associated with one of a plurality of previously executed branch instructions, each of said plurality of offsets specifying a location of said associated previously executed branch instruction within a line of said instruction cache selected by said fetch address, each of said plurality of direction predictions predicting whether said associated branch instruction will be taken or not taken, each of said plurality of valid indicators indicating whether said associated target address is a valid target address; and

branch control logic, coupled to said BTAC, for generating a selector signal in response to said fetch address and said plurality of offsets, direction predictions, and valid indicators, said selector signal selecting one of said plurality of target addresses provided by said BTAC as a subsequent fetch address on said address bus,

wherein said selector signal is used to select said one of said plurality of target addresses only if said associated valid indicator indicates that said target address is valid, only if said associated direction prediction predicts that said associated branch instruction will be taken, and only if said associated offset is greater than or equal to a predetermined plurality of least significant bits of said fetch address,

wherein if a plurality of said plurality of offsets is valid, taken, and greater than or equal to said portion of said fetch address, said selector signal is used to

select said one of said plurality of target addresses whose associated offset is a smallest of said plurality of said plurality of valid, taken offsets greater than or equal to said portion of the fetch address.

2. (currently amended) The microprocessor of claim 1, wherein said selected one of said plurality of target addresses is selected as said subsequent fetch address regardless of whether said associated previously executed branch instruction ~~one of said plurality of branch instructions associated with said selected one of said plurality of target addresses~~ is present in ~~a~~ said line of instructions in said instruction cache that is selected by said fetch address.

3. (canceled)

4. (canceled)

5. (currently amended) The microprocessor of claim 1, ~~4,~~ wherein said plurality of least significant bits of said fetch address specify a byte offset of said associated branch instruction within a line of said instruction cache selected by said fetch address.

6. (currently amended) The microprocessor of claim 1, ~~4,~~ wherein said plurality of least significant bits of said fetch address comprises a number of bits corresponding to a number of bits comprising said offset.

7. (canceled)

8. (canceled)

9. (canceled)

10. (canceled)

11. (canceled)

12. (original) The microprocessor of claim 1, further comprising:

address selection logic, coupled to said BTAC, for selecting said one of said plurality of target addresses as said subsequent fetch address in response to said selector signal.

13. (currently amended) An apparatus for selecting a target address for one of a plurality of previously executed branch instructions, said plurality of previously executed branch instructions being potentially present in a line of an instruction cache selected by a fetch address, the fetch address provided to the instruction cache on an address bus, the apparatus comprising:

a branch target address cache (BTAC), coupled to the address bus, configured to provide a plurality of target addresses cached therein ~~in response to~~ indexed by the fetch address, and to provide a corresponding plurality of offsets within the instruction cache line for each of the plurality of previously executed branch instructions;

control logic, coupled to said BTAC, for generating a selector in response to the fetch address and said offsets, said selector for selecting one of said plurality of target addresses, wherein said control logic generates said selector to select said one of said plurality of target addresses that has a smallest one of said corresponding plurality of offsets greater than or equal to a corresponding portion of the fetch address, if said BTAC indicates that the fetch address hit in said BTAC and that said one of said plurality of target addresses is a valid target address, and if said BTAC predicts that one of the plurality of branch instructions corresponding to said smallest said corresponding one of said plurality of offsets will be taken; and

address selection logic, coupled to the selector, for selecting one of said plurality of target addresses as a subsequent fetch address for the instruction cache in response to said selector, said address selection logic selecting said one of said plurality of target addresses as said subsequent fetch address for the instruction cache regardless of how many branch instructions are present in the instruction cache line selected by the fetch address.

14. (canceled)

15. (canceled)

16. (canceled)

17. (canceled)

18. (canceled)

19. (original) The apparatus of claim 13, wherein said BTAC provides said plurality of target addresses cached therein for a subset of the instruction cache line.

20. (original) The apparatus of claim 13, wherein said BTAC provides said plurality of target addresses prior to decoding of said instruction cache line.

21. (original) The apparatus of claim 13, wherein the fetch address is a virtual address, wherein said BTAC provides said plurality of target addresses based on the virtual fetch address without converting the virtual fetch address to a physical address.

22. (original) The apparatus of claim 13, wherein the plurality of previously executed branch instructions potentially present in the instruction cache line comprises a plurality of return instructions, wherein said plurality of offsets provided by said BTAC comprises offsets for said plurality of return instructions.

23. (original) The apparatus of claim 22, further comprising:

a call/return stack, coupled to said BTAC, for providing a return address to said address selection logic.

24. (original) The apparatus of claim 23, wherein said control logic is configured to generate said selector to selectively control said address selection logic to select said return address provided by said call/return stack in response to said plurality of offsets and the fetch address.

25. (currently amended) An apparatus for selecting a branch target address in a pipelined microprocessor having an instruction cache, a fetch address provided to the instruction cache on an address bus selecting a line of instructions therein, the apparatus comprising:

a branch target address cache (BTAC), coupled to the address bus, for providing information cached therein about a plurality of previously executed branch instructions ~~in response to~~ indexed by the fetch address, said information comprising a plurality of target addresses associated with said plurality of previously executed branch instructions; and

control logic, coupled to said BTAC, for selecting as a subsequent fetch address on the address bus one of said plurality of target addresses associated with one of said plurality of branch instructions, said subsequent fetch address selected in response to said information and the fetch address;

wherein said control logic selects said one of said plurality of target addresses that is valid, that is predicted taken, and that is first seen with respect to the fetch address, said one of said plurality of target addresses selected whether or not a branch instruction is present in the line of instructions.

26. (original) The apparatus of claim 25, wherein said control logic is configured to generate an indication that one of said plurality of target addresses provided by said BTAC was selected as said subsequent fetch address, wherein said indication is provided to an instruction buffer for receiving the line of instructions.

27. (original) The apparatus of claim 26, wherein said indication is provided to the instruction buffer for association with one of the instructions in the line of instructions, said one of the instructions presumably corresponding to said one of the plurality of branch instructions that is associated with said selected one of said plurality of target addresses.

28. (original) The apparatus of claim 27, wherein said indication is associated in the instruction buffer with said one of the instructions based on a location within the instruction cache line of said one of the plurality of branch instructions that is associated with said selected one of said plurality of target addresses, said location comprised in said information provided by said BTAC.

29. (currently amended) A method for selecting a fetch address to provide to an instruction cache for speculatively branching a microprocessor, the method comprising:

providing a plurality of target addresses and instruction cache line offsets of a corresponding plurality of previously executed branch instructions, in response to a first fetch address provided to the instruction cache;

providing a plurality of direction predictions, each of said plurality of direction predictions predicting whether a corresponding one of said plurality of previously executed branch instructions will be taken;

providing a plurality of valid indications, each of said plurality of valid indications indicating whether a corresponding one of said plurality of target addresses is a valid target address; and

~~determining, based on said plurality of offsets, which of said previously executed branch instructions is located after said first fetch address; and~~

selecting, as a second fetch address to provide to the instruction cache, in response to said ~~determining~~providing said plurality of target addresses, instruction cache line offsets, direction predictions, and valid indications, one of said plurality of target addresses corresponding to one of said branch instructions that is valid, predicted taken, located after said first fetch address, and ~~which is~~ nearest said first fetch address.

30. (original) The method of claim 29, wherein said selecting comprises selecting said second fetch address whether or not a branch instruction is present in a line of instructions in the instruction cache selected by said first fetch address.

31. (original) The method of claim 29, further comprising:

caching said plurality of target addresses and said instruction cache line offsets of said corresponding plurality of previously executed branch instructions prior to said providing.

32. (original) The method of claim 29, wherein said first and second fetch addresses are virtual addresses.

33. (original) The method of claim 29, wherein said plurality of previously executed branch instructions comprise x86 branch instructions.

34. (original) The method of claim 29, wherein said providing said plurality of target addresses comprises providing two target addresses per a subset of a line of instructions that is selected by said first fetch address.

35. (original) The method of claim 29, further comprising:

providing a plurality of direction predictions of said corresponding plurality of previously executed branch instructions in response to said first fetch address.

36. (canceled)

37. (canceled)

38. (canceled)